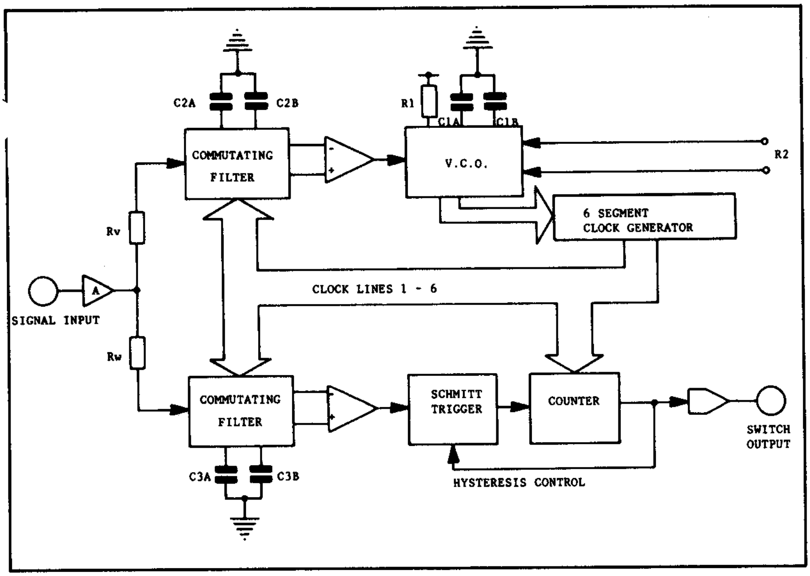
CML Semiconductor Products

PRODUCT INFORMATION

FX105P Tone Detector

Publication D/105/4 July 1994

Obsolete Product
- For Information Only -



FX105P

FEATURES

- OPERATES IN HIGH NOISE CONDITIONS
- ⩾40dB SIGNAL INPUT RANGE
- SIMULTANEOUS TONE DETECTION
- ADJUSTABLE BANDWIDTH
- HERMETICALLY SEALED CERAMIC PACKAGE
- WIDE FREQUENCY RANGE

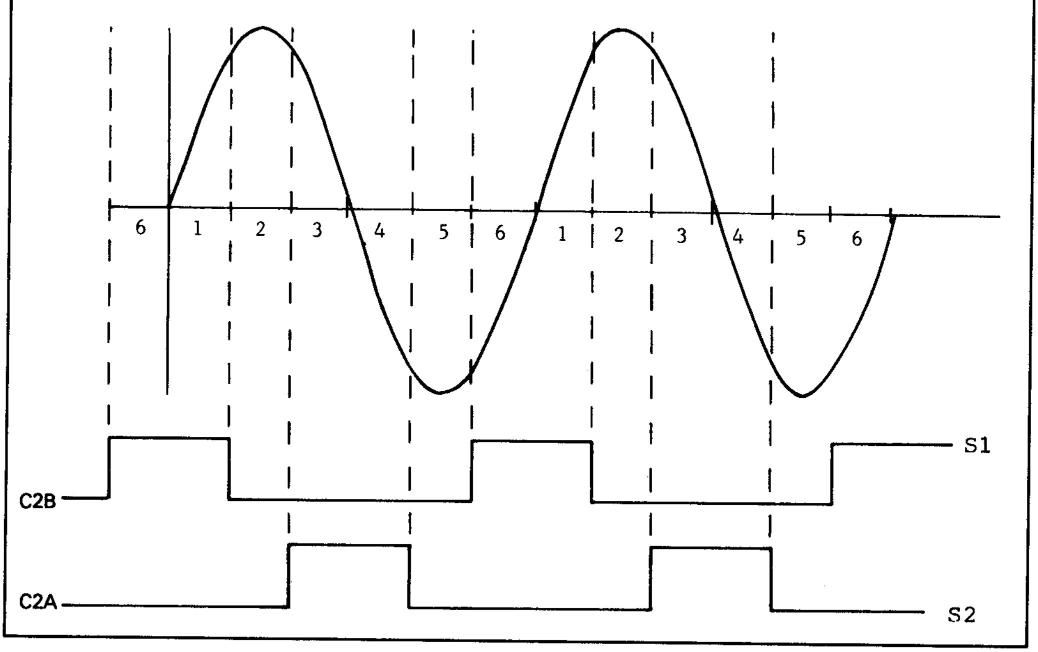
DESCRIPTION

The FX-105 is a monolithic tone operated switch, designed for tone decoding in single and multitone signalling systems.

The device employs decoding techniques which allow tones to be recognised in the presence of high noise levels or strong adjacent channel tones.

Tone channel centre frequency and channel bandwidth can each be adjusted independently. The circuit has a high noise immunity against harmonic and sub-harmonic responses and is able to maintain a constant bandwidth and high noise immunity over a wide range of input signal levels.

V.C.O. SAMPLING WAVEFORMS FIG. 2



METHOD OF OPERATION

Input signals are A.C. coupled to the buffer input, which is internally biased at 50% of supply voltage, the signal appears at the output of the buffer as an A.C. voltage superimposed on the D.C. bias level. The signal is then coupled via RV and RW to the voltage controlled oscillator and word sampling switches, which sequentially connect C2 and C3 into circuit to form four sample and hold RC integrators.

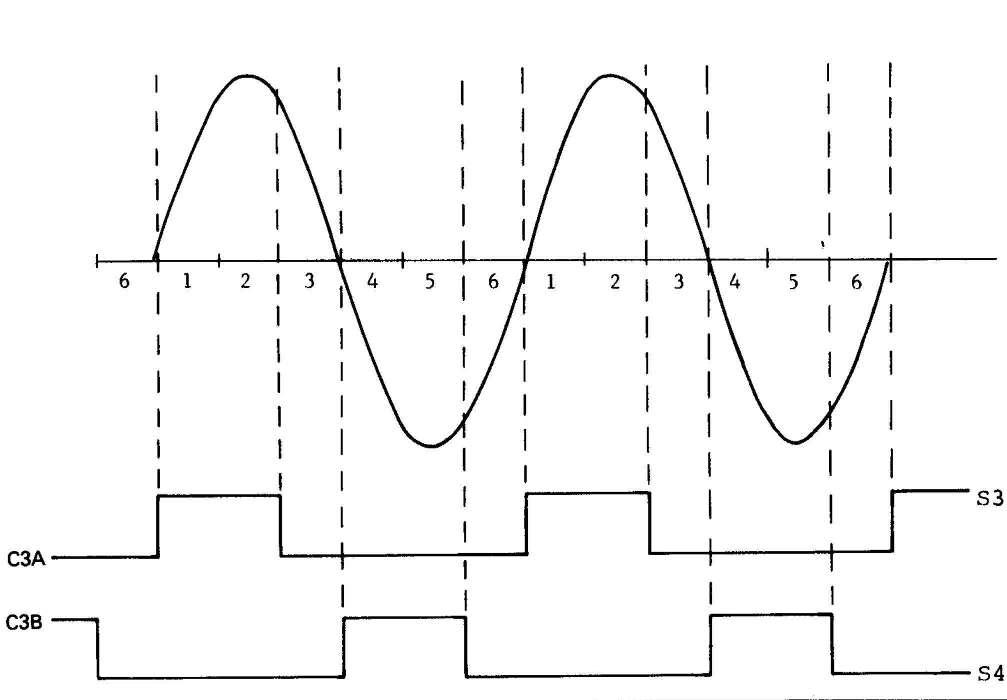
With no input signal, each capacitor charges to the D.C. bias level and differential voltages are zero. When an input signal is applied, each capacitor receives an additional charge according to the integrated average of the signal waveform during the interval the capacitor is switched into circuit.

Figure 2 above shows the operating sequence of the V.C.O. sampling switches and their phase relationship to a locked on inband signal. As can be seen from Figure 2 C2A and C2B should not receive any additional charge as they always sample the input as it crosses the D.C. bias level. Should the signal not be locked to the V.C.O. then a positive or negative charge voltage will appear on C2A or C2B, this voltage when differentially amplified is applied to the V.C.O. as an error correcting signal to enable the V.C.O. to achieve lock.

Figure 3 shows the operating sequence of the 'Word' sampling switches and their relationship to a locked on inband signal. As can be seen from Figure 3 the charge being applied to C3A should always be positive and the charge applied to C3B should always be negative with respect to the common bias level.

These capacitor potentials are differentially amplified and applied to a D.C. comparator, which switches at a predetermined threshold voltage. The comparator output is a logic signal used to control a counter which switches the FX-105 output ON when the comparator output is maintained in the 'Word Present' state for a minimum number of consecutive signal samples. The output switch reduces the comparator threshold by 50% when turned on, thereby introducing threshold hysterises which minimises output chatter with marginal input signal amplitudes.

WORD SAMPLING WAVEFORMS FIG. 3



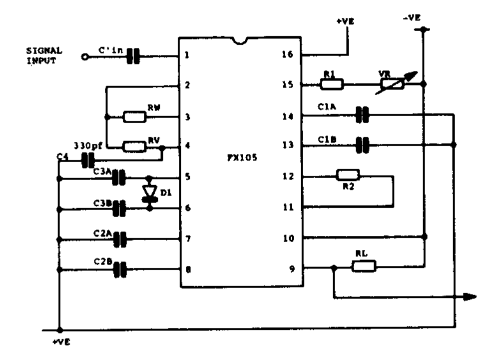
METHOD FOR CALCULATING EXTERNAL COMPONENT VALUES

The external components shown below in Figure 4 are used to adjust the various performance parameters of the FX-105. The signal to noise performance, turn on delay and signal bandwidth are all interrelated factors which should be optimised to meet the requirements of the application.

By selecting component values in accordance with the following graphs nominally optimum circuit performance is obtained for any given application.

FIG.4

FX105 EXTERNAL COMPONENT CONNECTIONS



The user should first define the following application parameters.

A. The centre frequency to be detected (f'o).

B. The FX-105 Minimum Usable Bandwidth (MUBW). This is obtained by taking into account the worst case tolerances on the input tone frequency and variations in the FX-105 f'o due to supply voltage (0.07%/%) and ambient temperature (0.02%/°C) changes.

C. The maximum permissible FX-105 response time.

D. The minimum input signal amplitude.

Using this information the appropriate component values can be calculated, and the signal to noise performance obtained may then be read from a chart.

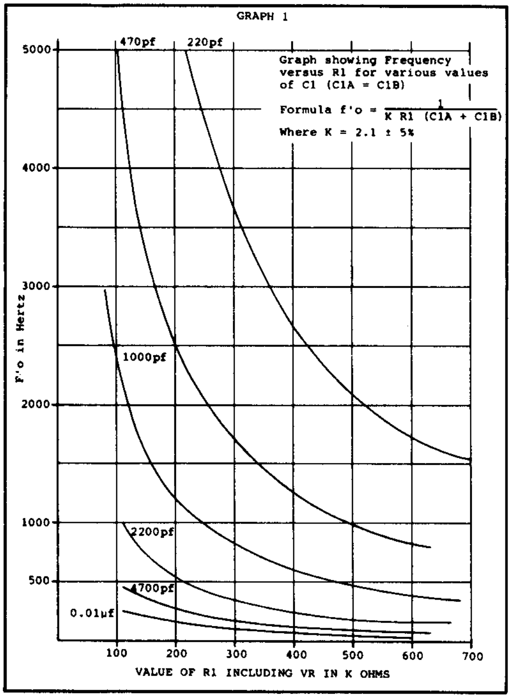
Using the graphs overleaf the following worked example may be used to calculate component values for any given application.

A. FX-105 centre band frequency (f'o) = 2800Hz.

B. FX-105 bandwidth = 6%.

C. FX-105 maximum response time = 50ms.

D. Minimum input signal amplitude = 200mVolts R.M.S.



R1 C1A C1B

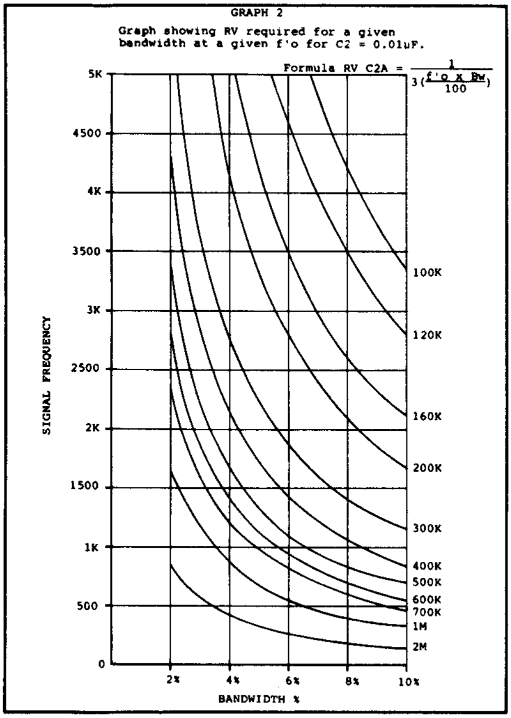
These components set the free running frequency of the V.C.O. and thereby the centre band frequency of the FX-105.

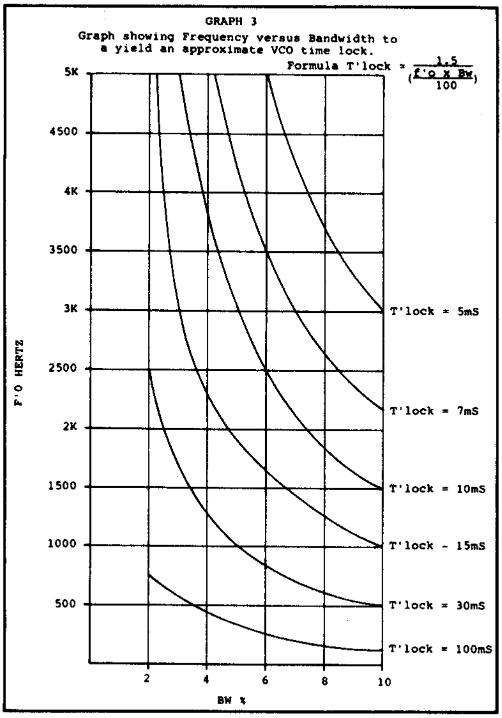
By using graph number 1 the frequency 2800Hz can be seen to correspond to a value of capacitor of 220 picofarads and a resistor value of 385k ohms, this resistance can be achieved with a 300k ohm fixed resistor for R1 and a 100k ohm potentiometer.

Graph number 2 shows that for a frequency of 2800Hz and a bandwidth of 6% a resistor RV of 200k ohms and a capacitance for C2A and C2B of 0.01 microfarads will be required.

The response time of the FX-105 is the sum of the V.C.O. 'Lock' time (T'lock) and the 'Word' integration time (T'word).

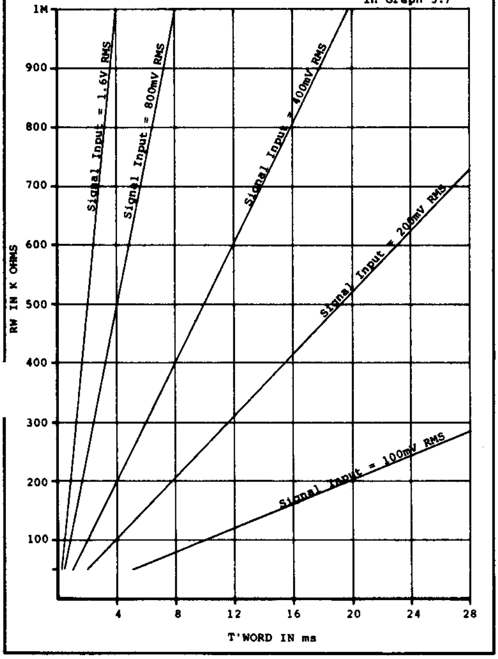
Graph number 3 shows that for a frequency of 2800Hz and a bandwidth of 6% the approximate 'Lock' time will be 9 milliseconds, as we have a maximum response time of 50 milliseconds, this allows for a 'Word' time of 41 milliseconds.





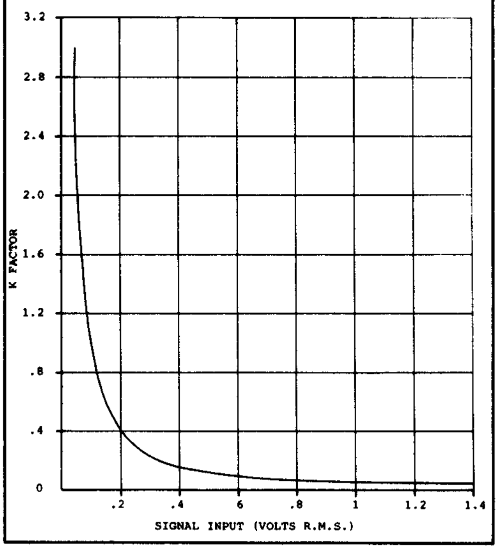
GRAPH 4

Graph showing RW required for T'word for a given signal input assuming C3A = C3B = 0.1uF. Formulae T'word = RwC3A x K(given in Graph 5.)



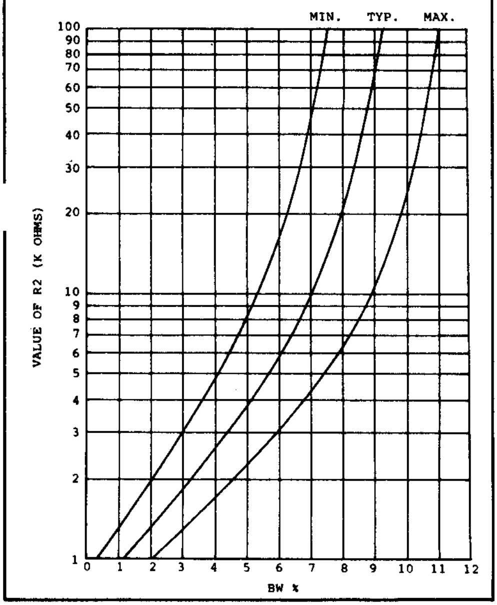
GRAPH 5

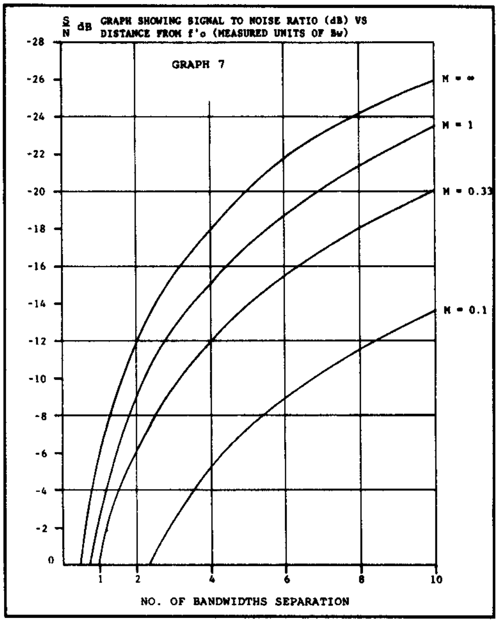
GRAPH SHOWING K FACTOR VS SIGNAL INPUT AMPLITUDE.



GRAPH 6

GRAPH SHOWING VALUE OF R2(KΩ) TO YIELD SELECTED BANDWIDTH(%)





Graph number 4 shows that for a signal amplitude of 200mVolts, a resistor value RW of 510k ohms with a 0.1 microfarad capacitor for C3A and B will yield a 'Word' time of 20ms. This will yield a response time of 9ms + 20ms = 29ms.

Graph 6 shows the range of values for R2 to yield a given bandwidth. The exact bandwidth given by any value of R2 will vary with differing production batches, therefore in applications where an exact bandwidth is required R2 should be a variable resistor which is adjusted on test.

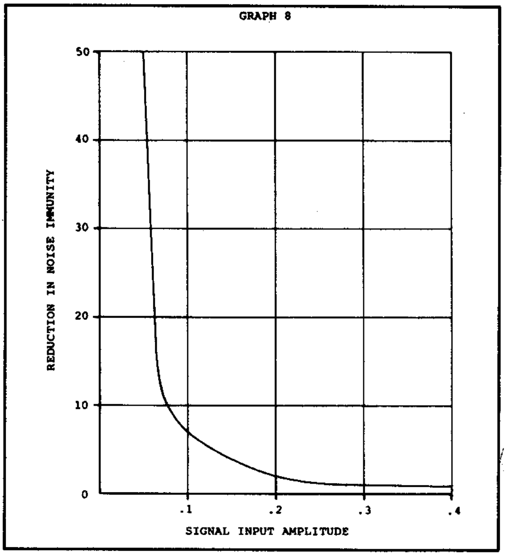
To calculate the worst case signal to noise ratio the FX-105 will work with the above component values. The formula is as follows:

$$M = \frac{f'o \times Bw}{100} \times (Rw\ C3A)$$

$$\therefore M = \frac{2800 \times 6}{100} \times (0.51M\Omega \times 0.1\mu F)$$

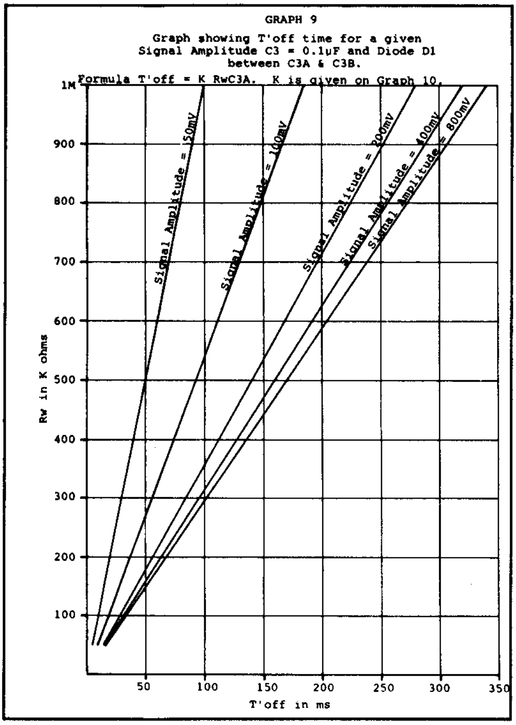
$$\therefore M = 168 \times 0.051$$

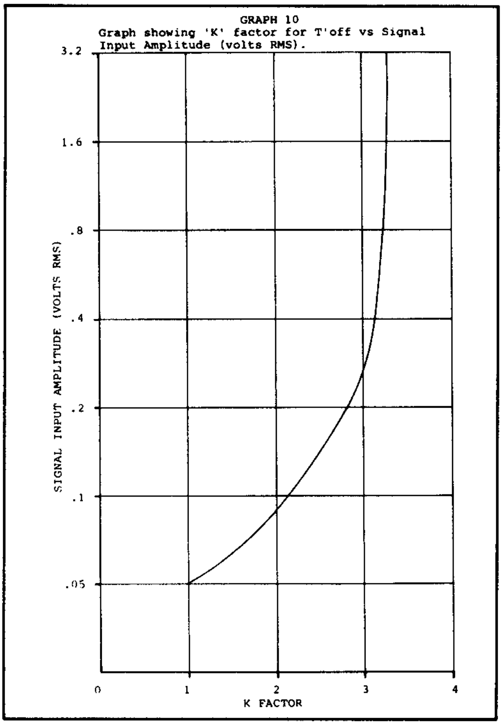
$$\therefore M \simeq 8.57$$



By substituting the value for M of 8.57 in graph number 7 the signal to noise ratio of an adjacent tone can be found, this then has to be decreased depending upon the tone amplitude. The figure to decrease SNR by is given in graph 8.

Graphs 9 and 10 show the approximate time the FX-105 will take to turn off after an inband signal has been removed. The turn off time is calculated with a diode (1N914 or similar) between pins 5 and 6 as shown in Figure 4. The effect of this diode is to greatly reduce the turn off time with signal input amplitudes greater than 300mV R.M.S.





FX105P Pin Functions

1	Signal Input	9	Switch Output
2	Buffer Output	10	V_{DD}
3	RW	11	HI
4	RV	12	LO
5	C3A	13	C1B
6	C3B	14	C1A
7	C2A	15	RI
8	C2B	16	V_{SS}

Due to the FX105's ability to decode tones in the presence of adjacent channel tones or noise, the device is ideally suited to applications where a number of tones are sequentially or simultaneously transmitted over a common link.
In the example shown below, a number of single-tone transmitters are transmitting over a common link (such as cable, o or optical) to a number of FX105P receivers. The transmitters may transmit either individually or simultaneously without the FX105P receivers missing or receiving a false call.

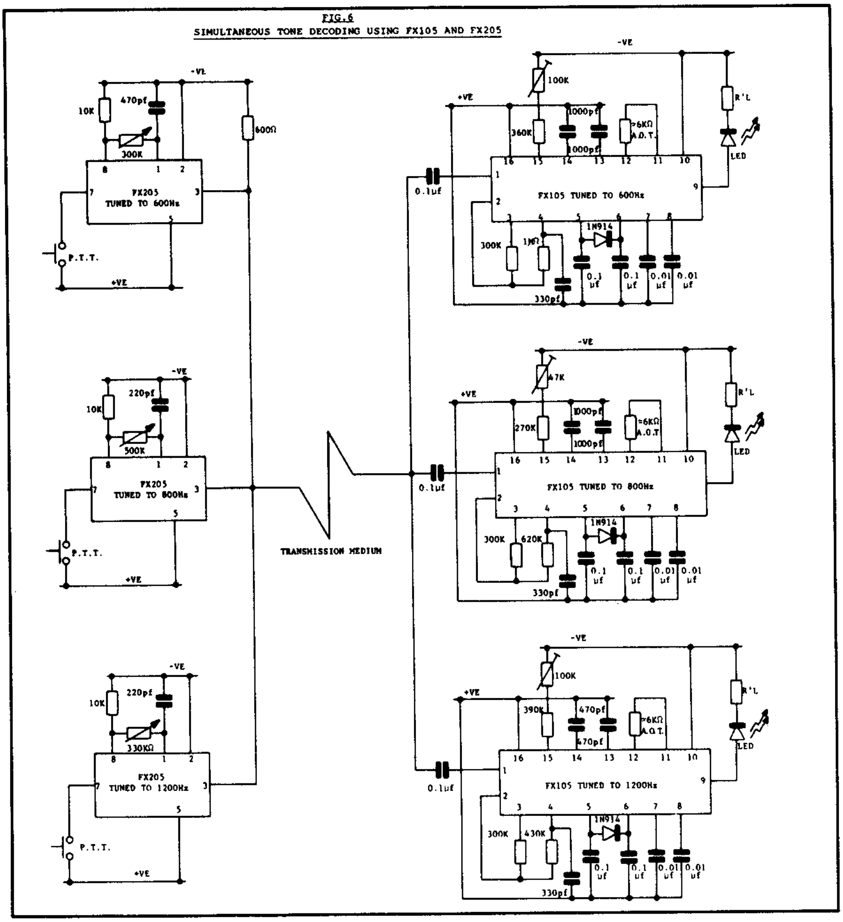


FIG.6
SIMULTANEOUS TONE DECODING USING FX105 AND FX205

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Input voltage between any pin and +ve supply	-20V and +0.3V
Total device dissipation @ T_{AMB} 20°C	400mW Max.
Operating temperature range: **FX105P**	-30°C to +85°C
Storage temperature range: **FX105P**	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 12.0V, T_{AMB} = 20°C. Due to ac signal coupling either supply may be 'ground'.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		10.0	12.0	15.0	V
Supply Current	1	-	5.0	-	mA
Input Impedance		-	200	-	kΩ
Signal Input	2, 3	0.055	-	5.0	V rms
Channel Frequency		0.04	-	5.0	kHz
Bandwidth		2.0	-	10.0	%
Output Switch Load Current		-	-	10.0	mA
Frequency Stabilty (with temperature)		-	0.02	-	%/°C
Frequency Stabilty (with supply voltage)		-	0.07	-	%/V

Notes

1. Supply current excluding load. Note maximum switch load current.
2. Signal-plus-noise range.
3. For signal input voltages greater than V_{DD} x 0.143, pins 1 and 2 should be open circuit and the signal applied via C_{IN} to the junction of RV and RW.

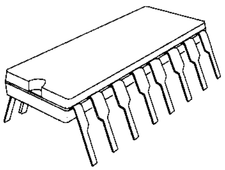
Package Outlines

The FX105P is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.

Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX105P 16-pin plastic DIL (P3)

NOT TO SCALE



Max. Body Length 19.24mm
Max. Body Width 6.41mm

Handling Precautions

The FX105P is a PMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

Ordering Information

FX105P 16-pin plastic DIL